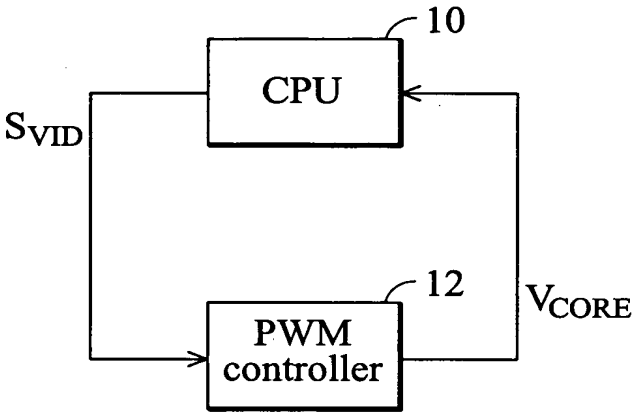
10
CPU
SVID
12
PWM controller
VCORE

FIG. 1

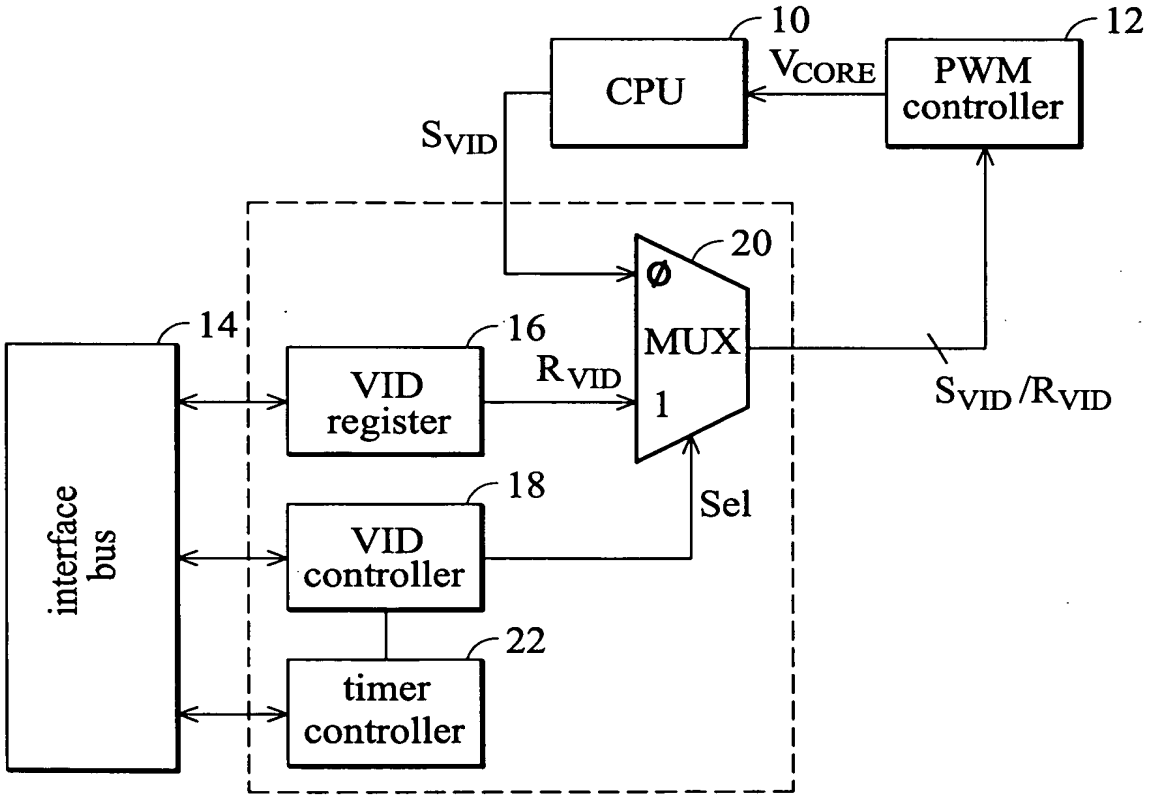
10
CPU
VCORE
12
PWM controller
SVID
20
Ø
MUX
1
14
16
RVID
VID register
SVID /RVID
interface bus
18
VID controller
Sel
22
timer controller

FIG. 2

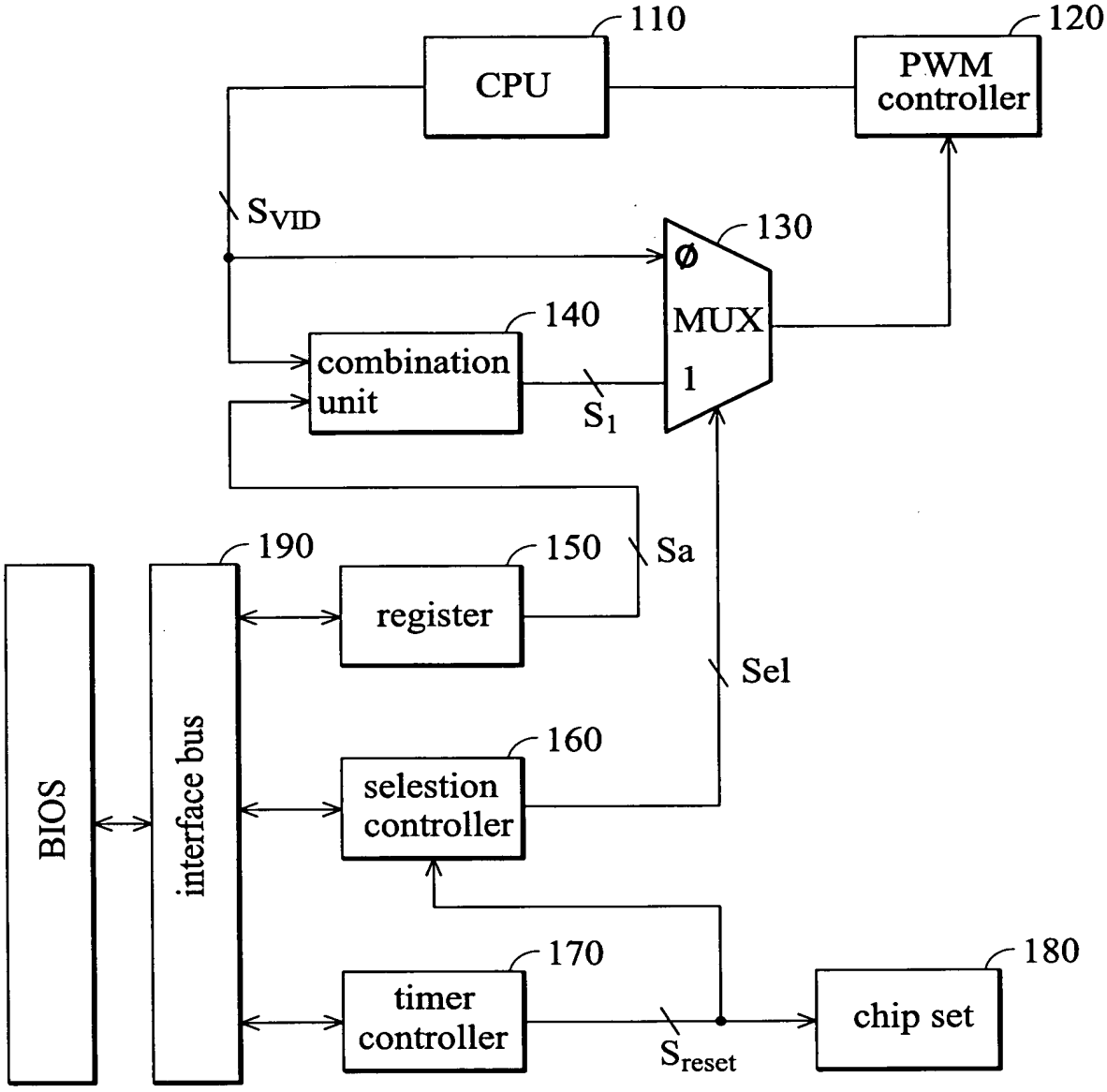
110
CPU
120
PWM controller
S_{VID}
130
Ø
MUX
1
140
combination unit
S_1
190
150
Sa
register
BIOS
interface bus
Sel
160
selestion controller
170
timer controller
S_{reset}
180
chip set
100

FIG. 3